Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L8	14	(("5563527") or ("5696455") or ("6172519") or ("5572715") or ("5428571") or ("5982683") or ("5548228")).PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/12/12 08:09
L9	71	"5563527" "5696455" "6172519" "5572715" "5428571" "5982683" "5548228"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/12 08:01
L10	2	("5696455").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/12/12 08:02
L15	4	(("5563527") or ("6963222")).PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/12/12 09:52
L19	2827	(tunnel adj diode)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/12 09:54
L20	41	19 and (access adj transistor)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/12 09:54
L21	21	20 and capacitor	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/12 09:54
L22	4	21 and PLD	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/12 09:54
S1	292	NON$VOLATILE adj MEMORY adj CELL and LATCH same integrated	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 15:44
S2	2360	NON$VOLATILE adj MEMORY adj CELL and LATCH	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/09/10 22:44
S3	56	NON$VOLATILE adj MEMORY adj CELL same LATCH same integrated	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/09/10 22:44
S4	27	NON$VOLATILE adj MEMORY adj CELL with LATCH with integrated	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/09/10 22:44

S5	2	Young-Phillip.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 15:46
S6	0	Paak-Sunhom.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 15:45
S7	17745	programmable adj logic adj device	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 17:06
S8	319	S7 and NON$VOLATILE adj MEMORY adj CELL	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 15:48
S9	31	S8 and latch near3 circuit	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 17:00
S10	4	S9 and initial$7 near2 circuit	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 17:06
S11	2	S9 and initial$7 adj circuit	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 16:59
S12	11	S9 and initial$7	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 16:08
S13	3	S12 and switch$6 adj2 circuit	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 15:54
S14	4	S9 and initialization	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 16:48
S15	2	S10 and initialization	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 15:58
S16	7	S12 and voltage near3 supply	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 16:09

S17	2	S12 and voltage adj supply	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 16:09
S18	7	S9 and power$up	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 16:55
S19	2	S18 and initialization	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 16:49
S20	4	(("5272368") or ("5563527")).PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/12/05 16:50
S21	44	"5272368" "5563527"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 16:50
S22	4	S21 and programmable adj logic adj device and power$up and latch and initial$7	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 16:51
S23	7	(US-6449197-$ or US-5572715-$ or US-5982683-$ or US-5563527-$ or US-5696455-$).did. or (US-6118693-$ or EP-515039-$).did.	USPAT; DERWENT	OR	ON	2005/12/05 16:52
S24	1	power$up near2 initialization near2 cycle and programmable adj logic adj device	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 16:59
S25	1	"6963222"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 16:58
S26	2555	xilinx.as.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 16:58
S27	1363	S26 and programmable adj logic adj device	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/12 08:10
S28	1	S27 and power$up near2 initialization near2 cycle	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 17:04

S29	18	S27 and initial$7 adj circuit	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 17:00
S30	3	S29 and latch near3 circuit	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 17:00
S31	4	S9 and logic adj core	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 17:01
S32	5	S9 and logic near2 core	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/12 07:58
S33	248	NON$VOLATILE near2 memory adj cell same latch same (pass gate or transfer gate)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 17:05
S34	18	S33 and programmable adj logic adj device	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 17:07
S35	1	S34 and initial$7 near2 circuit	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/12/05 17:06